

IN THE CLAIMS:

Please amend claims 25, 33, and 39 as follows:

E1 (sub F1) 25. (Three times amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:
a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;
at least one p-well and at least one n-well on said substrate first surface;
at least one p-type area within said at least one n-well;
at least one n-type area within said at least one p-well; and
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate.

E2 (sub F2) 33. (Amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:
a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;
at least one p-well and at least one n-well on said substrate first surface;
at least one doped area within at least one of said at least one n-well and said at least one p-well;
and
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate.

E3 (sub F3) 39. (Amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:
a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;
at least one first doped area on said substrate first surface;

E3
and

at least one second, differently doped area within said at least one first doped area; and
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface
and said second surface of said semiconductor substrate.

Please add the following new claims:

- E4*
and F4 →
46. A pre-anneal intermediate structure useful in the formation of electrical device isolation structures, comprising:
a semiconductor substrate that is free of field oxide structures and includes a first surface and a second surface, said first surface opposing said second surface;
at least one p-well and at least one n-well defined on said first surface of said substrate;
at least one p-type area defined within said at least one n-well;
at least one n-type area defined within said at least one p-well; and
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.
47. The pre-anneal intermediate structure of claim 46 further comprising a layer of oxide between said first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.
48. The pre-anneal intermediate structure of claim 46, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon nitride.
49. The pre-anneal intermediate structure of claim 46, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon oxynitride.